iSBC 108A/116A™ COMBINATION MEMORY AND I/O EXPANSION BOARDS

8K or 16K bytes of read/write memory (iSBC 108A™, iSBC 116A™ boards respectively).

Sockets for up to 32K bytes of EPROM.

Auxiliary power bus and memory protect control logic provided for battery backup RAM requirements.

RAM and EPROM assignable anywhere within a one megabyte address space.

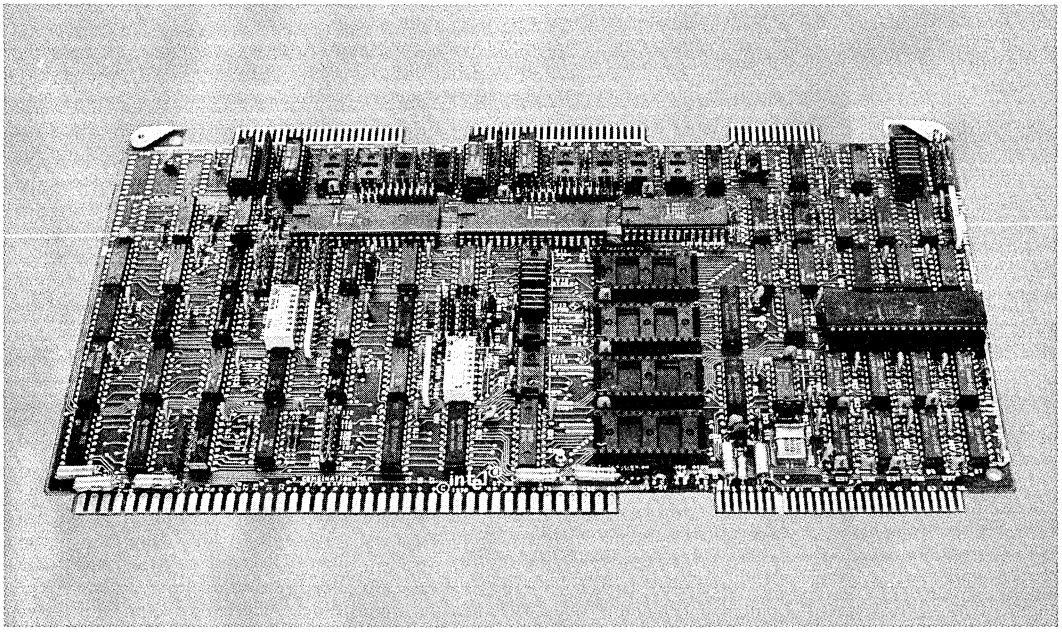
48 programmable I/O lines with sockets for interchangeable line drivers and terminators.

Synchronous/asynchronous communications interface with RS232C drivers and receivers.

Eight maskable interrupt request lines with a pending interrupt register.

1 msec interval timer.

The iSBC 108A and iSBC 116A Combination Memory and I/O Boards are members of Intel's complete line of iSBC memory and I/O expansion boards. Both boards interface directly with any iSBC 80, iSBC 86 or iSBC 88 single board computer via the MULTIBUS interface to expand RAM, EPROM, serial I/O and parallel I/O capacity. This mixture makes the iSBC 108A and 116A combination boards ideal for small microcomputer systems where the on-board resources of a single board computer are insufficient for incrementing the memory and I/O capacities of larger multiple board systems.



FUNCTIONAL DESCRIPTION

Memory Capabilities

The iSBC 108A board contains 8K bytes and the iSBC 116A board contains 16K bytes of RAM implemented with eight dynamic RAM components. An Intel 8202A dynamic RAM controller is used to provide all timing, control and refresh signals. Starting on a 4K byte boundary, RAM may be located anywhere in the MULTIBUS one megabyte memory address space.

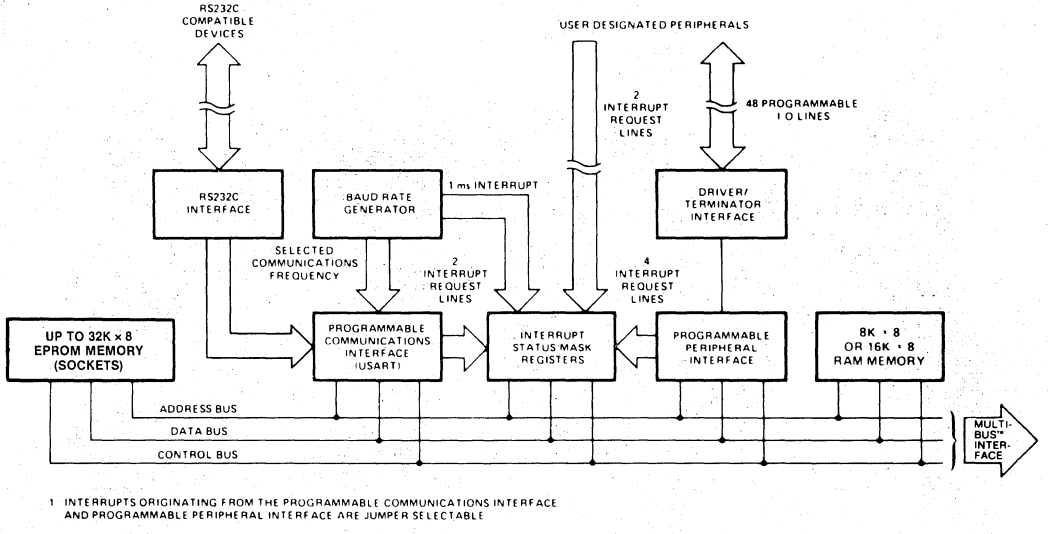
Both combination boards contain four 28-pin sockets for adding up to 4K bytes (using Intel 2708 or 2758 EPROMs), 8K bytes (using Intel 2716 EPROMs), 16K bytes (using Intel 2732 or 2732A EPROMs), or 32K bytes (using Intel 2764 EPROMs) of non-volatile read-only-memory.

Parallel I/O Interface

Each combination board contains 48 programmable I/O lines implemented using two Intel 8255A programmable peripheral interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output, and bi-directional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, round, or woven cable.

Communications Interface

A programmable communications interface using Intel's 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on each board. A jumper selectable baud rate generator provides the USART with all common communications frequencies between 75 Hz and 38.4 kHz. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and asynchronous serial transmission rate are all under program con-



1 INTERRUPTS ORIGINATING FROM THE PROGRAMMABLE COMMUNICATIONS INTERFACE AND PROGRAMMABLE PERIPHERAL INTERFACE ARE JUMPER SELECTABLE

Figure 1. iSBC 108A/116A™ Combination Memory and I/O Expansion Board Block Diagram

trol. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of a comprehensive RS232C interface on the boards in conjunction with the USART provides a direct interface to CRTs, RS232C compatible cassettes, and asynchronous and synchronous modems. The RS232C, serial data lines, and signal ground lines are brought out to a 26-pin edge connector which mates with RS232C compatible flat or round cables.

Interrupt Request Lines

Interrupt requests may originate from eight sources. Four jumper selectable interrupt requests can be automatically generated by the programmable peripheral interfaces when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). Two interrupt request lines may be interfaced directly from user designated peripheral devices via the I/O edge connector. An on-board register contains the status of all eight interrupt request lines, and may be interrogated by the CPU. Each interrupt request line is maskable under program control. Routing for the eight interrupt request lines is jumper selectable. They may be ORed to provide a single interrupt request line for the iSBC 80/10A, or they may be individually provided to the MULTIBUS interface for use by the other iSBC single board computers.

Interval Timer

Each board contains a jumper selectable 1 ms interval timer. The timer is enabled by jumpering one of the interrupt request lines from the I/O edge connector to a 1 ms interval interrupt request signal originating from the baud rate generator.

Table 1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X[2]
	4	X		X			X[2]

Notes

1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output or port 1 is used as a bidirectional port.

2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output or port 4 is used as a bidirectional port.

SPECIFICATIONS

Memory Word Size
8 bits only. 16-bit single board computers may use this memory only for the storage of 8-bit data.

Memory Addressing
EPROM — Up to 4K, 8K, 16K or 32K bytes of read-only-memory may be located anywhere within a one megabyte address range. The base address must be located on a 4K byte boundary. EPROM addresses may not cross 32K byte boundaries.

RAM — 8K (iSBC 108A) or 16K (iSBC 116A) bytes of RAM may be located anywhere in a one megabyte address range. The base address must be located on a 4K byte boundary. RAM addresses may not cross 32K byte boundaries.

Memory Response Time

Memory	Access (ns)	Cycle (ns)
RAM	450 max*	580 max*
EPROM/ROM	450 max	635 max

* Without refresh contention.

I/O Transfer Rate
Parallel — Read or write acknowledge time 575 ns max.

Serial — (USART)

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷ 16	÷ 64
307.2	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

Serial Communications Characteristics
Synchronous — 5 — 8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5 — 8 bit characters; break characters generation; 1, 1½, or 2 stop bits; false start bit detectors.

Interrupts
Eight interrupt request lines may originate from the programmable peripheral interface (4 lines), the USART (2 lines) or user specified devices via the I/O edge connector (2 lines), or interval timer.

Interrupt Register Addresses
XX1 Interrupt mask register
XX0 Interrupt status register

Note
XX is any two hex digits assigned by jumper selection.

Timer Interval
1.003 ms ±0.1% when 110 baud rate is selected.
1.042 ms ±0.1% for all other baud rates.

Interfaces
Bus — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Serial I/O — RS232C
Interrupt Requests — All TTL compatible

Connectors

Interface	No. of Pins	Centers (in.)	Mating Connectors
Bus (P1)	86	0.156	Viking 3KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Aux. Power (P2)	60	0.1	AMP PE5-14559 or TI H311130

NOTE: Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM packaging.

I/O Addressing

Port	1	2	3	4	5	6	8255A No. 1 Control	8255A No. 2 Control	USART Data	USART Control
Address	XX4	XX5	XX6	XX8	XX9	XXA	XX7	XXB	XXC or XXE	XXD or XXF

Note
XX is any two hex digits assigned by jumper selection.

Auxiliary Power
An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect
An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

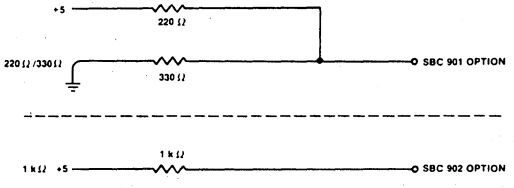
Line Drivers and Terminators

I/O Drivers — The following line drivers and terminators are all compatible with the I/O driver sockets on the iSBC 108A/116A board. Ports 1 and 4 have 25 mA totem-pole drivers and 1 kΩ terminators.

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note
I = inverting; NI = non-inverting; OC = open collector.

I/O Terminators — 220Ω/330Ω divider or 1 kΩ pullup.



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	32
Commands	Tri-State	32

Physical Characteristics
Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 14 oz (397.3 gm)

Electrical Characteristics
Average DC Current

	V_{DD} = +12±5%	V_{CC} = +5±5%	V_{BB} = -5±5%	V_{AA} = -12±5%
No EPROM or Terminators	250 mA	2.9 A	—	70 mA
4 2708s and 8 Terminators	520 mA	3.6 A	180 mA	70 mA
4 2716s and No Terminators	250 mA	3.3 A	—	70 mA
4 2732s and No Terminators	250 mA	3.5 A	—	70 mA
Aux. Power RAM Accessed	175 mA	0.45 A	3 mA	—
Aux. Power No RAM Access	20 mA	0.45 A	3 mA	—

Environmental Characteristics
Operating Temperature — 0°C to +55°C.

Reference Manuals
9800862 — iSBC 108A/116A Board Hardware Reference Manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 108A	Combination Memory and I/O Expansion Board with 8K bytes RAM
SBC 116A	Combination Memory and I/O Expansion Board with 16K bytes RAM