

Embedded Intel® 855GME GMCH to Intel® 852GM GMCH Design Respin

Application Note

September 2006



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Revision History

| Revision Number | Description | Revision Date |
|------------------------|--|----------------------|
| 002 | Changed "migration" to respin; updated Intel brand names | September 2006 |
| 001 | Initial release. | August 2006 |



1 Introduction

This document details the ability of existing designs integrating the Intel® 82855GME GMCH to scale down to the value segment using the Intel® 82852GM GMCH. It will only be suitable for designs derived from the Embedded Platform Design Guide that use the Intel® 82801DB I/O Controller Hub.

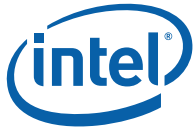
The Intel® 82855GME GMCH and Intel® 82852GM GMCH are very similar in form and function. This similarity makes the requirements of a design respin relatively simple. This document will show system designers the significant design changes that are required to migrate an Intel® 82855GME GMCH based design to an Intel® 82852GM GMCH based design.

1.1 Terminology

For this document, the following terminology applies

- *855GME* refers to the Intel® 82855GME GMCH
- *852GM* refers to the Intel® 82852GM GMCH
- *ICH4* refers to the Intel® 82801DB I/O Controller Hub
- *Celeron M processor* refers to both the Intel® Celeron® M processor and the Ultra Low Voltage Intel® Celeron® M processor
- *Pentium M processor* refers to both the Intel® Pentium® M processor and the Intel® Pentium® M processor on the 90 nm Process with 2-MB L2 Cache

| Term | Description |
|-------|--|
| ADD | AGP Digital Display |
| AGP | Accelerated Graphics Port |
| DDR | Double Data Rate |
| DVO | Digital Video Out |
| ECC | Error Correcting Code |
| FCBGA | Flip Chip Ball Grid Array |
| FSB | Front Side Bus – Processor to GMCH Interface |
| GMCH | Graphics Memory Controller Hub |



| Term | Description |
|------|--------------------|
| ICH | I/O Controller Hub |
| MB | Megabyte |
| MHz | Megahertz |
| ULV | Ultra Low Voltage |
| V | Volts |

1.2 Reference Documents

| Document | Document No./Location |
|---|---|
| Intel® 855GM/GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet | http://developer.intel.com/design/chipsets/datashts/252615.htm |
| Intel® 855GM/GME Chipset Graphics and Memory Controller Hub (GMCH) Specification Update | http://developer.intel.com/design/chipsets/specupdt/253572.htm |
| Intel(R) 855GME Chipset Graphics and Memory Controller Hub (GMCH) Specification Update Addendum | http://developer.intel.com/design/intarch/specupdt/274004.htm |
| Intel(R) 855GME Chipset and Intel(R) 82801DB (ICH4) I/O Controller Hub Embedded Platform Design Guide | http://developer.intel.com/design/intarch/designgd/273903.htm |
| Intel® 852GM/852GMV Chipset Graphics and Memory Controller Hub (GMCH) Datasheet | http://developer.intel.com/design/mobile/datashts/252407.htm |
| Intel® 852GM/852GMV Chipset Graphics and Memory Controller Hub (GMCH) Specification Update | http://developer.intel.com/design/chipsets/specupdt/253038.htm |
| Intel® 852GM Chipset and Intel® 82801DB I/O Controller Hub (ICH4) Embedded Platform Design Guide | http://developer.intel.com/design/intarch/designgd/309944.htm |



2 Features Comparison

This chapter will compare the various features and related specifications for the various interfaces and controllers where they differ between the 852GM and 855GME. The reader should assume that any interfaces and controllers that do not appear in this Chapter are identical in feature and specification.

2.1 Processor Interface

[Table 1](#) compares the various features and specification of the 855GME and the 852GM GMCHs relating to the processor interface.

Table 1. Process Interface

| Feature | Specification | |
|--------------------------------|---|--|
| | 852GM | 855GME |
| Supported Processors | <ul style="list-style-type: none"> Intel Celeron® Processor on 0.13 Micron Process in 478-Pin Package Mobile Intel Celeron® Processor on 0.13 Micron Process in Micro-FCPGA Package Celeron M Processor ULV Celeron M Processor | <ul style="list-style-type: none"> Pentium M Processor Pentium M Processor on 90 nm process with 2 MB L2 cache Celeron M Processor ULV Celeron M Processor Celeron M Processor on 90 nm process |
| Nominal FSB Signalling Voltage | <ul style="list-style-type: none"> 1.05 V: Celeron M processor 1.3 V: All other processors | <ul style="list-style-type: none"> 1.05 V: All processors |



2.2 Memory Support

[Table 2](#) compares the various features and specification of the 855GME and the 852GM GMCHs relating to the memory interface.

Table 2. Memory Support

| Feature | Specification | |
|------------------|---|--|
| | 852GM | 855GME |
| Memory Frequency | <ul style="list-style-type: none">• DDR200• DDR266 | <ul style="list-style-type: none">• DDR200• DDR266• DDR333 |
| ECC Support? | No | Yes ¹ |

NOTES:

1. ECC is not supported when AGP interface is active
2. DDR333 is only available if Vcc = 1.35 V

2.3 Graphics Support

[Table 3](#) compares the various features and specification of the 855GME and the 852GM GMCHs relating to the graphics interface.

Table 3. Graphics Support

| Feature | Specification | |
|------------------------|---|--|
| | 852GM | 855GME |
| Display Core Frequency | <ul style="list-style-type: none">• 133 MHz | <ul style="list-style-type: none">• 133 MHz• 200 MHz• 250 MHz ¹ |
| Number of DVO Port | One - DVOC | Two - DVOB and DVOC |
| AGP Support | No | Yes |

NOTES:

1. 250 MHz clock is only available if Vcc = 1.35 V



2.4 ICH Support

[Table 4](#) compares the various features and specification of the 855GME and the 852GM GMCHs relating to the ICHs it may support.

Table 4. ICH Support

| Feature | Specification | |
|------------------------|---------------|--------|
| | 852GM | 855GME |
| Validated with ICH4 | Yes | Yes |
| Validated with 6300ESB | No | Yes |

2.5 Power Supply

[Table 5](#) compares the various features and specification of the 855GME and the 852GM GMCHs relating to the power supply.

Table 5. Power Supply

| Feature | Specification | |
|-----------------------------|---|--|
| | 852GM | 855GME |
| Supply Voltage ¹ | <ul style="list-style-type: none"> • 1.2 V | <ul style="list-style-type: none"> • 1.2 V • 1.35 V ² |

NOTES:

1. VCC, VCCADPLLA, VCCADPLLB, VCCAGPLL, VCCAHPPLL, VCCASM, VCCHL
2. Required for DDR333 and/or 250MHz Graphics



3 Pinout Comparison

Table 6 highlights any differences between the pinout of the 852GM and 855GME. If a pin is not listed in Table 6 then it should be assumed that the function of the pin is identical between the 852GM and 855GME.

Table 6. Pin Functional Differences

| Pin # | Signal Name | | Functional Difference | |
|-------|-------------|---|---------------------------------|---|
| | 852GM | 855GME | 852GM | 855GME |
| C2 | RSVD | GST[2] | Reserved | Multiplexed <ul style="list-style-type: none"> • Strapping Signal • AGP Status Signal |
| D5 | DPMS | <ul style="list-style-type: none"> • GPIPE# • DPMS | Display Power Management Signal | Multiplexed <ul style="list-style-type: none"> • Display Power Management Signal • AGP Pipelined Read |
| E2 | ADDID[3] | <ul style="list-style-type: none"> • GSBA3 • ADDID[3] | ADD Card ID | Multiplexed <ul style="list-style-type: none"> • ADD Card ID • AGP Sideband Address |
| E3 | ADDID[2] | <ul style="list-style-type: none"> • GSBA2 • ADDID[2] | ADD Card ID | Multiplexed <ul style="list-style-type: none"> • ADD Card ID • AGP Sideband Address |
| E5 | ADDID[0] | <ul style="list-style-type: none"> • GSBA0 • ADDID[0] | ADD Card ID | Multiplexed <ul style="list-style-type: none"> • ADD Card ID • AGP Sideband Address |
| F4 | ADDID[5] | <ul style="list-style-type: none"> • GSBA5 • ADDID[5] | ADD Card ID | Multiplexed <ul style="list-style-type: none"> • ADD Card ID • AGP Sideband Address |
| F5 | ADDID[1] | <ul style="list-style-type: none"> • GSBA1 • ADDID[1] | ADD Card ID | Multiplexed <ul style="list-style-type: none"> • ADD Card ID • AGP Sideband Address |



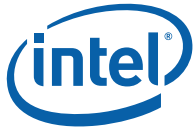
| Pin # | Signal Name | | Functional Difference | |
|-------|-------------|---|-------------------------------|---|
| | 852GM | 855GME | 852GM | 855GME |
| F6 | ADDID[7] | <ul style="list-style-type: none"> GSBA7 ADDID[7] | ADD Card ID | Multiplexed <ul style="list-style-type: none"> ADD Card ID AGP Sideband Address |
| G2 | DVOBCINTR# | <ul style="list-style-type: none"> GAD30 DVOBCINTR# | DVOBC Interrupt | Multiplexed <ul style="list-style-type: none"> DVOBC Interrupt AGP Address/Data |
| G3 | DVOCD[11] | <ul style="list-style-type: none"> GAD28 DVOCD[11] | DVOC Data | Multiplexed <ul style="list-style-type: none"> DVOC Data AGP Address/Data |
| G5 | ADDID[4] | <ul style="list-style-type: none"> GSBA4 ADDID[4] | ADD Card ID | Multiplexed <ul style="list-style-type: none"> ADD Card ID AGP Sideband Address |
| G6 | ADDID[6] | <ul style="list-style-type: none"> GSBA6 ADDID[6] | ADD Card ID | Multiplexed <ul style="list-style-type: none"> ADD Card ID AGP Sideband Address |
| H1 | DVOCD[7] | <ul style="list-style-type: none"> GAD24 DVOCD[7] | DVOC Data | Multiplexed <ul style="list-style-type: none"> DVOC Data AGP Address/Data |
| H2 | DVOCD[6] | <ul style="list-style-type: none"> GAD25 DVOCD[6] | DVOC Data | Multiplexed <ul style="list-style-type: none"> DVOC Data AGP Address/Data |
| H3 | DVOCD[8] | <ul style="list-style-type: none"> GAD27 DVOCD[8] | DVOC Data | Multiplexed <ul style="list-style-type: none"> DVOC Data AGP Address/Data |
| H4 | DVOCD[9] | <ul style="list-style-type: none"> GAD26 DVOCD[9] | DVOC Data | Multiplexed <ul style="list-style-type: none"> DVOC Data AGP Address/Data |
| H5 | DVOCFLDSTL | <ul style="list-style-type: none"> GAD31 DVOCFLDSTL | TV Field and Flat Panel Stall | Multiplexed <ul style="list-style-type: none"> TV Field and Flat Panel Stall AGP Address/Data |
| H6 | DVOCD[10] | <ul style="list-style-type: none"> GAD29 | DVOC Data | Multiplexed |



| Pin # | Signal Name | | Functional Difference | |
|-------|-------------|--|---------------------------------------|---|
| | 852GM | 855GME | 852GM | 855GME |
| | | <ul style="list-style-type: none"> DVOCD[10] | | <ul style="list-style-type: none"> DVOC Data AGP Address/Data |
| J2 | DVOCCLK# | <ul style="list-style-type: none"> GADSTB#1 DVOCCLK# | Complementary Differential DVOC Clock | Multiplexed <ul style="list-style-type: none"> Complementary Differential DVOC Clock AGP Address/Data Strobe 1 Complement |
| J3 | DVOCCLK | <ul style="list-style-type: none"> GADSTB1 DVOCCLK | Complementary Differential DVOC Clock | Multiplexed <ul style="list-style-type: none"> Complementary Differential DVOC Clock AGP Address/Data Strobe 1 |
| J5 | DVOCD[5] | <ul style="list-style-type: none"> GCB#3 DVOCD[5] | DVOC Data | Multiplexed <ul style="list-style-type: none"> DVOC Data AGP Command/Byte Enable |
| J6 | DVOCD[4] | <ul style="list-style-type: none"> GAD23 DVOCD[4] | DVOC Data | Multiplexed <ul style="list-style-type: none"> DVOC Data AGP Address/Data |
| K1 | DVOCD[1] | <ul style="list-style-type: none"> GAD20 DVOCD[1] | DVOC Data | Multiplexed <ul style="list-style-type: none"> DVOC Data AGP Address/Data |
| K2 | DVOCD[3] | <ul style="list-style-type: none"> GAD22 DVOCD[3] | DVOC Data | Multiplexed <ul style="list-style-type: none"> DVOC Data AGP Address/Data |
| K3 | DVOCD[2] | <ul style="list-style-type: none"> GAD21 DVOCD[2] | DVOC Data | Multiplexed <ul style="list-style-type: none"> DVOC Data AGP Address/Data |
| K5 | DVOCD[0] | <ul style="list-style-type: none"> GAD19 DVOCD[0] | DVOC Data | Multiplexed <ul style="list-style-type: none"> DVOC Data AGP Address/Data |
| K6 | DVOCHSYNC | <ul style="list-style-type: none"> GAD17 DVOCHSYNC | DVOC Horizontal Sync | Multiplexed <ul style="list-style-type: none"> DVOC Horizontal Sync AGP Address/Data |



| Pin # | Signal Name | | Functional Difference | |
|-------|-------------|--|-----------------------------------|--|
| | 852GM | 855GME | 852GM | 855GME |
| K7 | MI2CCLK | <ul style="list-style-type: none"> GIRDY# MI2CCLK | DVO I2C Clock | Multiplexed <ul style="list-style-type: none"> DVO I2C Clock AGP Initiator Ready |
| L2 | RSVD | <ul style="list-style-type: none"> GCBE# DVOBBLANK# | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Blank AGP Command/Byte Enable |
| L3 | DVOCBLANK# | <ul style="list-style-type: none"> GAD18 DVOCBLANK# | DVOC Blank | Multiplexed <ul style="list-style-type: none"> DVOC Blank AGP Address/Data |
| L5 | DVOCVSYNC | <ul style="list-style-type: none"> GAD16 DVOCVSYNC | DVOC Vertical Sync | Multiplexed <ul style="list-style-type: none"> DVOC Vertical Sync AGP Address/Data |
| L7 | DVODETECT | <ul style="list-style-type: none"> GPAR DVODETECT | DVO Detect | Multiplexed <ul style="list-style-type: none"> DVO Detect AGP Parity |
| M1 | RSVD | <ul style="list-style-type: none"> GAD12 DVOBD[10] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data AGP Address/Data |
| M2 | RSVD | <ul style="list-style-type: none"> GAD14 DVOBFLDSTL | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB TV Field and Flat Panel Stall AGP Address/Data |
| M3 | DVOBCCLKINT | <ul style="list-style-type: none"> GAD13 DVOBCCLKINT | DVOBC Pixel Clock Input/Interrupt | Multiplexed <ul style="list-style-type: none"> DVOBC Pixel Clock Input/Interrupt AGP Address/Data |
| M5 | RSVD | <ul style="list-style-type: none"> GAD11 DVOBD[11] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data AGP Address/Data |
| M6 | MDVIDATA | <ul style="list-style-type: none"> GFRAME# MDVIDATA | DVI DDC Data | Multiplexed <ul style="list-style-type: none"> DVI DDC Data AGP Frame |
| N2 | RSVD | <ul style="list-style-type: none"> GAD10 DVOBD[8] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data |



| Pin # | Signal Name | | Functional Difference | |
|-------|-------------|--|-----------------------|--|
| | 852GM | 855GME | 852GM | 855GME |
| | | | | <ul style="list-style-type: none"> AGP Address/Data |
| N3 | RSVD | <ul style="list-style-type: none"> GAD9 DVOBD[9] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data AGP Address/Data |
| N5 | RSVD | <ul style="list-style-type: none"> GAD8 DVOBD[6] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data AGP Address/Data |
| N6 | MI2CDATA | <ul style="list-style-type: none"> GDEVSEL# MI2CDATA | DVO I2C Data | Multiplexed <ul style="list-style-type: none"> DVO I2C Clock AGP Device Select |
| N7 | MDVICLK | <ul style="list-style-type: none"> GTRDY# MDVICLK | DVI DDC Clock | Multiplexed <ul style="list-style-type: none"> DVI DDC Clock AGP Target Ready |
| P2 | RSVD | <ul style="list-style-type: none"> GCBE#0 DVOBD[7] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data AGP Command/Byte Enable |
| P3 | RSVD | <ul style="list-style-type: none"> GADSTB0 DVOBCLK | Reserved | Multiplexed <ul style="list-style-type: none"> Differential DVOB Clock AGP Address/Data Strobe 0 |
| P4 | RSVD | <ul style="list-style-type: none"> GADSTB#0 DVOBCLK# | Reserved | Multiplexed <ul style="list-style-type: none"> Differential DVOB Clock Complement AGP Address/Data Strobe 0 Complement |
| P5 | RSVD | <ul style="list-style-type: none"> GAD6 DVOBD[5] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data AGP Address/Data |
| P6 | RSVD | <ul style="list-style-type: none"> GAD7 DVOBD[4] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data AGP Address/Data |
| P7 | MDDCCLK | <ul style="list-style-type: none"> GSTOP# MDDCCLK | DVI DDC Clock | Multiplexed <ul style="list-style-type: none"> DVI DDC Clock |



| Pin # | Signal Name | | Functional Difference | |
|-------|-------------|---|-------------------------|--|
| | 852GM | 855GME | 852GM | 855GME |
| | | | | <ul style="list-style-type: none"> AGP Stop |
| R3 | RSVD | <ul style="list-style-type: none"> GAD3 DVOBD[0] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data AGP Address/Data |
| R4 | RSVD | <ul style="list-style-type: none"> GAD4 DVOBD[3] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data AGP Address/Data |
| R5 | RSVD | <ul style="list-style-type: none"> GAD2 DVOBD[1] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data AGP Address/Data |
| R6 | RSVD | <ul style="list-style-type: none"> GAD5 DVOBD[2] | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Data AGP Address/Data |
| T5 | RSVD | <ul style="list-style-type: none"> GAD1 DVOBVSNC | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Horizontal Sync AGP Address/Data |
| T6 | RSVD | <ul style="list-style-type: none"> GAD0 DVOBHSNC | Reserved | Multiplexed <ul style="list-style-type: none"> DVOB Vertical Sync AGP Address/Data |
| T7 | MDDCDATA | <ul style="list-style-type: none"> GAD15 MDDCDATA | DVI DDC Data | Multiplexed <ul style="list-style-type: none"> DVI DDC Data AGP Address/Data |
| AG14 | SDQ[64] | SDQ[64] | No Connect ¹ | Memory Data Line ² |
| AE14 | SDQ[65] | SDQ[65] | No Connect ¹ | Memory Data Line ² |
| AE17 | SDQ[66] | SDQ[66] | No Connect ¹ | Memory Data Line ² |
| AG16 | SDQ[67] | SDQ[67] | No Connect ¹ | Memory Data Line ² |
| AH14 | SDQ[68] | SDQ[68] | No Connect ¹ | Memory Data Line ² |
| AE15 | SDQ[69] | SDQ[69] | No Connect ¹ | Memory Data Line ² |
| AF16 | SDQ[70] | SDQ[70] | No Connect ¹ | Memory Data Line ² |



| Pin # | Signal Name | | Functional Difference | |
|-------|-------------|---------|-------------------------|---------------------------------|
| | 852GM | 855GME | 852GM | 855GME |
| AF17 | SDQ[71] | SDQ[71] | No Connect ¹ | Memory Data Line ² |
| AD15 | SDQS[8] | SDQS[8] | No Connect ¹ | Memory Data Strobe ² |
| AH15 | SDM[8] | SDM[8] | No Connect ¹ | Memory Data Mask ² |

NOTES:

1. Signals only required for ECC memory. ECC error detection is not supported on 852GM.
2. Signals only required for ECC memory.



4 Package Comparison

855GME and 852GM share identical 732-ball Micro-FCBGA packages. As a result, 852GM should be drop-in compatible with an 855GME as far as thermal, mechanical and layout design is concerned.



5 Implementation Differences

The design guidelines for 852GM and 855GME are very similar and, as a result, an 855GME design requires relatively limited alteration to use the 852GM instead.

5.1 Processor Support

Chapter [2.1](#) lists the processors that have been validated with the 852GM and 855GME. The only processor that is validated with both GMCHs is the Intel® Celeron® M processor. An 855GME to 852GM design respin should use the Celeron M processor.

The design guidelines for Celeron M processor and Pentium M processor with 855GME are identical. These guidelines are also suitable for the 852GM meaning that no schematic or layout redesign should be necessary.

5.2 Memory Support

Chapter [2.2](#) lists the differences in validated memory support between the 852GM and 855GME.

Since 852GM does not support ECC error detection, an 855GME to 852GM design respin should ensure that the following memory interface signals are left as No Connect:

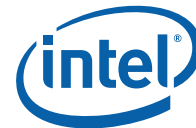
- SDQ[71:64]
- SDQS[8]
- SDM[8]

Aside from the difference stated above, the memory interface design guidelines for 855GME and 852GM are identical meaning that no schematic or layout redesign should be necessary.

5.3 Graphics Support

Chapter [2.3](#) lists the differences in the Graphics controller and associated interfaces between 855GME and 852GM.

Since the 852GM does not support either the DVOB or AGP interfaces, an 855GME to 852GM design respin should ensure that the graphics interfaces signals are connected in the correct manner. The correct connection depends on the configuration of the graphics interface. Chapters [5.3.1](#) and [5.3.2](#) cover the two most common configurations.



5.3.1 855GME with AGP Slot

Although 852GM does not support the AGP interface, the AGP slot can still be used to support ADD (AGP Digital Display) cards that connect to the DVOC interface.

The following signals should be No Connect:

- DVOBD[11:0]
- DVOBHSYNC, DVOBVSYNC
- DVOBBLANK#
- DVOBFLDSTL
- GST[2]

The following signals should be re-routed to match the guidelines in the 852GM PDG:

- GST[1:0]
- PIPE#/DPMS

5.3.2 855GME with DVO Down

If the design implements a DVO transmitter on the motherboard then the following signals should be No Connect:

- DVOBD[11:0]
- DVOBHSYNC, DVOBVSYNC
- DVOBBLANK#
- DVOBFLDSTL
- GST[2]

5.4 ICH Support

Chapter [2.4](#) lists the I/O Controller Hubs that have been validated with the 852GM and 855GME. The only ICH that is validated with both GMCHs is the ICH4. An 855GME to 852GM design respin should use the ICH4.

The design guidelines for using ICH4 with 855GME and 852GM are identical, meaning that no schematic or layout redesign should be necessary



5.5 Power Supply

Chapter 2.5 lists the differences in power supply requirements between 855GME and 852GM. An 855GME to 852GM design respin should ensure that the following power balls are connected to a 1.2 V supply

- VCC
- VCCADPLLA, VCCADPLLB
- VCCAGPLL, VCCAHPLL
- VCCASM
- VCCHL

The decoupling requirements for these balls do not change between a 1.35 V or 1.2 V supply.

5.6 Reference Signals

Certain reference signals are dependent on the value of the GMCH’s core supply voltage. Table 7 indicates which signals are affected and how the design guidelines vary.

Table 7: Reference Signals

| Pin # | Signal Name | Termination | | |
|-------|---------------------|---|---|---|
| | | 852GM | 855GME 1.2V Supply ² | 855GME 1.35V Supply ² |
| T2 | HLRCOMP | 27.4 Ω 1% pull-up | 27.4 Ω 1% pull-up | 37.4 Ω 1% pull-up |
| U2 | PSWING ¹ | <ul style="list-style-type: none"> • R10 = 49.9 Ω ± 1% • R11 = 100 Ω ± 1% | <ul style="list-style-type: none"> • R10 = 49.9 Ω ± 1% • R11 = 100 Ω ± 1% | <ul style="list-style-type: none"> • R10 = 68.1 Ω ± 1% • R11 = 100 Ω ± 1% |
| W1 | HLVREF ¹ | <ul style="list-style-type: none"> • R8 = 243 Ω ± 1% • R9 = 100 Ω ± 1% | <ul style="list-style-type: none"> • R8 = 243 Ω ± 1% • R9 = 100 Ω ± 1% | <ul style="list-style-type: none"> • R8 = 287 Ω ± 1% • R9 = 100 Ω ± 1% |

NOTES:

1. Only relevant if using Individual HIVREF and HI_VSWING Voltage Reference Divider Circuits – See Figure 1 – for the ICH4 and GMCH.
2. VCC, VCCADPLLA, VCCADPLLB, VCCAGPLL, VCCAHPLL, VCCASM, VCCHL.

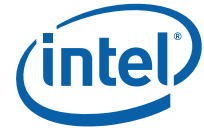
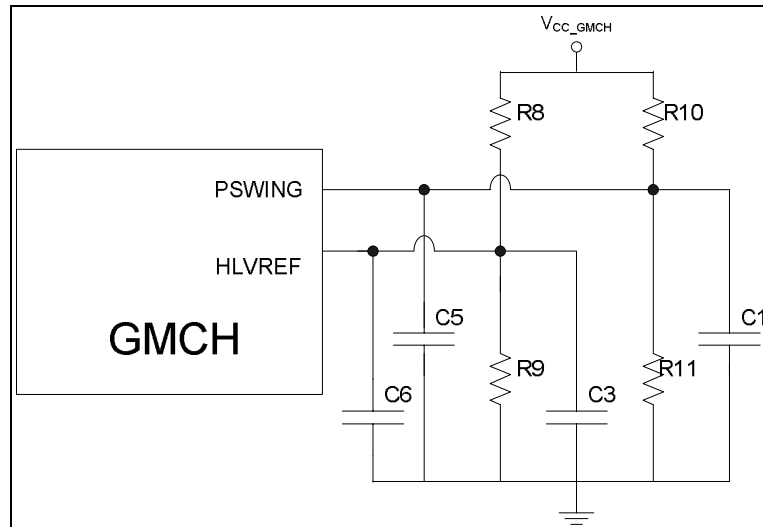


Figure 1: Individual HIVREF¹ and HI_VSWING² Voltage Reference Divider Circuits



NOTES:

1. HIVREF is 82801DB signal naming used in PDG. It is equivalent to the HLVREF GMCH signal.
2. HI_VSWING is 82801DB signal naming used in PDG. It is equivalent to the PSWING GMCH signal.