3 Volt Intel® StrataFlash™ Memory to MPC8260 PowerQUICC II* CPU Design Guide

Application Note 715

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Contents

Revision History

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08/05/99	-001	Original version
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1.0 Introduction

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memories with faster read times and a page-mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory's interface to the MPC8260 PowerQUICC II* microprocessor

This application note was written with preliminary information about 3 Volt Intel StrataFlash memory. Any changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0 Hardware Interface

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC}: Device power supply. 2.7 V – 3.6 V

V_{CCQ}: Output buffer power supply. This voltage controls the device's output voltages. 5 V ± 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

$CE_{0:2}$: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash memory components without additional decoding. For all designs in this document, CE_1 and CE_2 are tied to ground. CE_0 is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page-mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page-mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

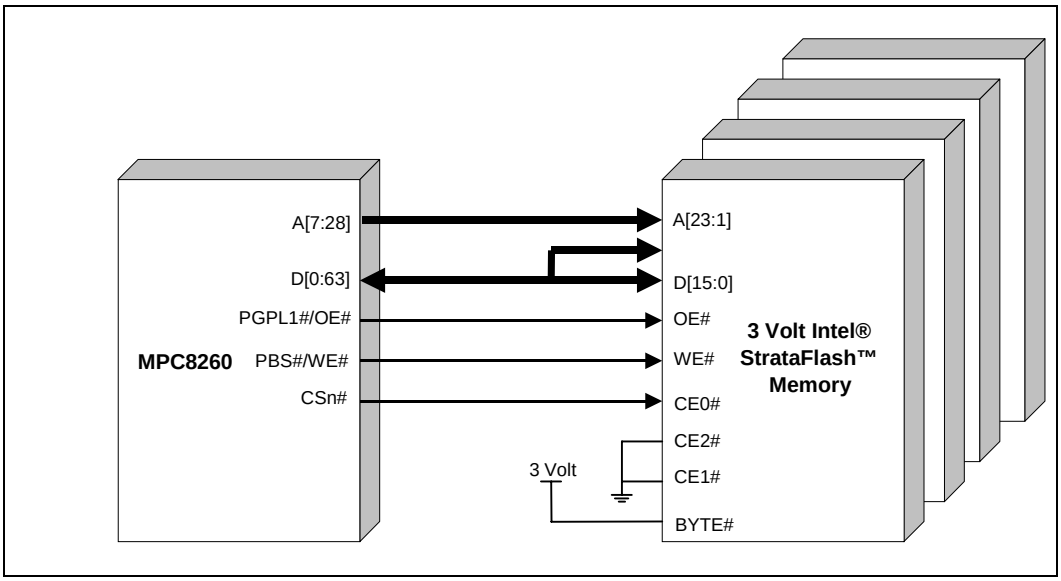
This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

All interfaces in this document use page-mode timings. Before 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set using the Set Read Configuration Register command. For more information on the RCR bits see the *3 Volt Intel® StrataFlash™ Memory:28F128J3A, 28F640J3A, 28F320J3A* datasheet.

3.0 Interfacing 3 Volt Intel® StrataFlash™ to the MPC8260 PowerQUICC II* at 66 MHz

The PowerQUICC II MPC8260 is a high quality processor used in telecommunications and networking market or other embedbed applications. This microprocessor can operate at a bus frequency of 66 MHz with four-word burst capability in x64 mode. Figure 1 illustrates the block diagram of the 3 Volt Intel StrataFlash memory interfaces to the MPC8260 processor.

Figure 1. 3 Volt Intel® StrataFlash™ Memory/MPC8260 Interface



3.1 Interface Considerations

This sample interface uses four 3 Volt Intel StrataFlash memory devices in 16-bit mode. Timing diagrams were made with the 64-Mbit 3 Volt Intel StrataFlash memory with the memory bus running at 66 MHz. There is no other required logic between the processor and the 3 Volt Intel StrataFlash memory.

This reference interface in this document uses page mode timings. Before 3 Volt Intel StrataFlash memory's page mode timings can be used, read configuration register bit 16 (RCR.16) must be set to b'1 to enable the page mode feature.

3.2 Processor Interface Signals

The sample reference uses the following main signals provided by the MPC8260 processor:

A[0-31]: The address bus signals the memory which piece of information is to be accessed.

D[0-63]: The data bus contains bi-directional data paths to transfer data between the processor and the flash memory.

CSn#: The Chip Select signal indicates which memory bank the processor is accessing.

GPL1# The General Purpose Line 1 Signal is the output enable to active the device's outputs during a read operation. This signal must remain inactive during a write operation.

BS#: The Byte Select is the write enable to active the low signal that controls during the write operation. BS# must remain inactive during read access.

3.3 Control Signal Generation

The MPC8260 processor controls the 3 Volt Intel StrataFlash memory CE# signals with CSn#. The OE# and WE# are controlled by the microprocessor's GPL1# and BSn# signals respectively. The signal timings are controlled by programming one of the processor's User Programmable Machine (UPM) table. These values can be found in the back of this note. The words 0x00h to 0x07h are the value for single read cycle. The words 0x08h to 0x17h are used to control burst read. The following words are used to control single write and burst write. To enable UPM control, the processor base register bit (BR[24:26]) must be set to b'100 if using UPMA. Similarly, the bit (BR[24:26]) must be set to b'101 if the designer uses UPMB and b'110 if using UPMC.

Figure 2 shows a four-word page mode read timing diagram. CSn# and GPL1# signal are set by programming one of the processor's UPM table. In order to read the UPM table correctly, the processor Machine X Mode Register's Read Loop Field (MMR[14:17]) must be set to b'0011 for active the processor four-word bursts.

Figure 2. 3 Volt Intel® StrataFlash™ Memory/MPC8260 Four-Word Page Mode Read Cycle at 66 MHz

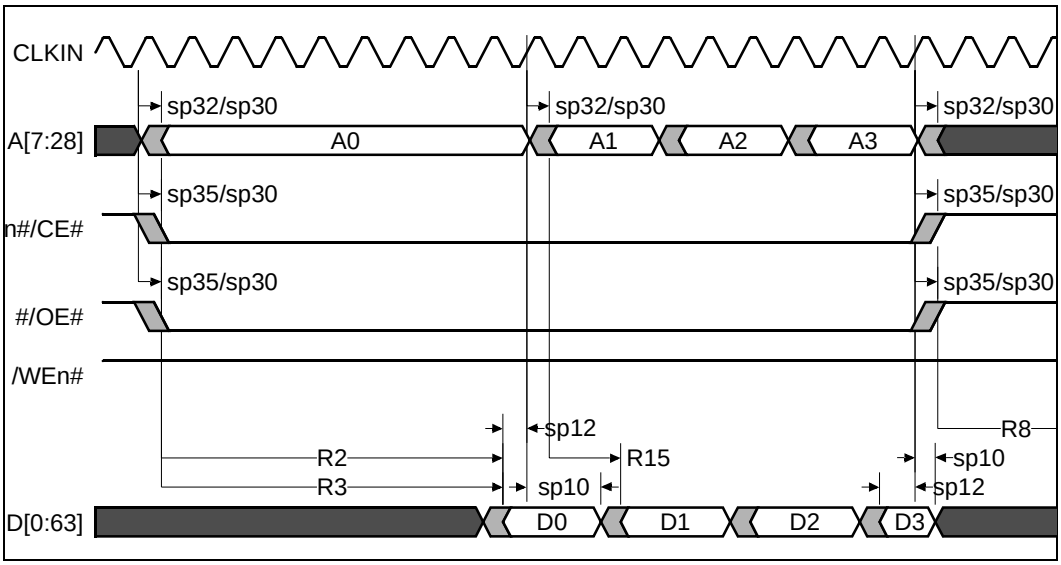
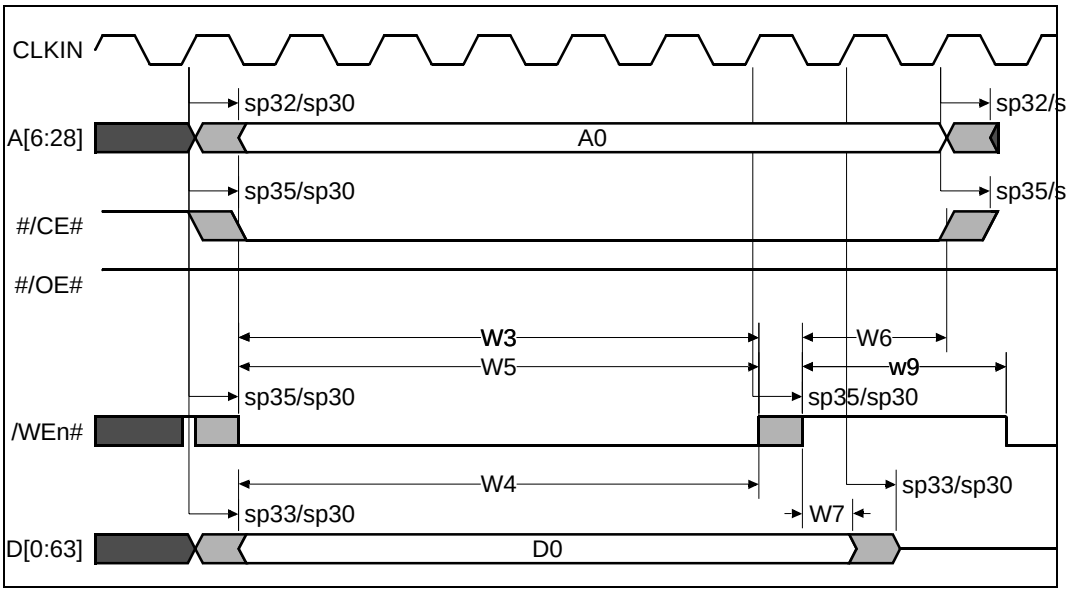


Figure 3 shows a write timing diagram. The processor's BSn# signal as controlled by the UPM can be directly used as WE#. The 3 Volt Intel StrataFlash memory does not support burst write. To disable bursts during write operations, the processor's UPM table must be programmed accordingly.

Figure 3. 3 Volt Intel® StrataFlash™ Memory/MPC8260 Write Cycle at 66 MHz



The following signal can be located in the *MPC8260 PowerQUICC II* ADS User's Manual* sp32/ sp30, sp35/sp30, sp33/sp30, sp10/sp12 timing.

The following signal can be found from the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, and 28F320J3A* datasheet: R2, R3, R8, R15, W3, W4, W5, W9 timing.

Read all appropriate documentation before attempting this interface.

4.0 Summary

The 3 Volt Intel StrataFlash Memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page-mode reads. The 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different Vccq voltages. The 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. This "glueless" interface reduce power consumption. 3 Volt Intel StrataFlash memory is an excellent option for code and data applications where high density and low cost are required.

Appendix A Additional Information

Order Number	Document/Tool
290667	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A* datasheet
298130	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A Specification Update*
297859	*AP-677 Intel® StrataFlash™ Memory Technology*
292222	*AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture*
292221	*AP-663 Using the Intel® StrataFlash™ Memory Write Buffer*
292218	*AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292172	*AP-617 Additional Flash Data Protection Using V_{PP} RP#, and WP#*
Note 4	*MPC8260 PowerQUICC II* ADS User's Manual*

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at http://developer.intel.com/design/flash/isf.
4. This manual can be located at the following URL:http://www.mot.com/SPS/RISC/cgi-bin/ncsp/ncsp.cgi.

Appendix B UPM Table Values

These are the values that the MPC8260's User Programmable Machine (UPM) controls the CSn#, GPL1# and BS#. In order to take advantage of the processor's feature using burst mode, the following values are calculated from the *MPC8260 PowerQUICC II User's Manual* (section 10). The words 0x00 to 0x07 are used to control single read. The words 0x08 to 0x17 are used to control the read timing using page mode. The words 0x18 to 0x1F are used to control the single write timing. The words 0x20 to 0x2F are used for write burst however the Intel StrataFlash memory does not support burst write.

Read Single Beat Cycle

UPM 0x00	0FF3EC00
UPM 0x01	0FF3EC00
UPM 0x02	0FF3EC80
UPM 0x03	0FF3EC80
UPM 0x04	0FF3EC80
UPM 0x05	0FF3E380
UPM 0x06	FFFFEC00
UPM 0x07	FFFFEC00

Read Burst Cycle (3 Volt Intel StrataFlash memory supports page mode)

UPM 0x08	0FF3EC00
UPM 0x09	0FF3EC00
UPM 0x0A	0FF3EC00
UPM 0x0B	0FF3EC00
UPM 0x0C	0FF3EC00
UPM 0x0D	0FF3EC00
UPM 0x0E	0FF3EC00
UPM 0x0F	0FF3EC00
UPM 0x10	0FF3E380
UPM 0x11	0FF3EC84
UPM 0x12	0FF3EC48
UPM 0x13	0FF3EC48
UPM 0x14	0FF3EC84
UPM 0x15	FFFFEC00
UPM 0x16	FFFFEC00
UPM 0x17	FFFFEC00

Write Single Beat Cycle

UPM 0x18	00FFEC00
UPM 0x19	00FFEC00
UPM 0x1A	00FFEC00
UPM 0x1B	00FFEC00
UPM 0x1C	00FFEC00
UPM 0x1D	00FFEC00
UPM 0x1E	0FFFEC07
UPM 0x1F	0FFFEC00

Write Burst Cycle

UPM 0x20	00FFEC00
UPM 0x21	00FFEC00
UPM 0x22	00FFEC00
UPM 0x23	00FFEC00
UPM 0x24	00FFEC00
UPM 0x25	00FFEC00
UPM 0x26	0FFFEC07
UPM 0x27	0FFFFC00
UPM 0x28	0FFFFC00
UPM 0x29	0FFFFC00
UPM 0x2A	0FFFFC00
UPM 0x2B	0FFFFC00
UPM 0x2C	0FFFFC00
UPM 0x2D	0FFFFC00
UPM 0x2E	0FFFFC00
UPM 0x2F	0FFFFC00