3 Volt Intel® StrataFlash™ Memory to Philips MIPS PR31700 CPU Design Guide

Application Note 709

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Contents

Revision History

Date of Revision	Version	Description
07/20/99	-001	Original version
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1.0 Introduction

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memories with faster read times and a page mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory's interface to the Philips MIPS-based PR31700 Poseidon processor

This application note was written with preliminary information about 3 Volt Intel StrataFlash memory. Any changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0 Hardware Interface

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC}: Device power supply. 2.7 V – 3.6 V

V_{CCQ}: Output buffer power supply. This voltage controls the device's output voltages. 5 V ± 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

$CE_{0:2}$: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash memory components without additional decoding. For all designs in this document, CE_1 and CE_2 are tied to ground. CE_0 is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

All interfaces in this document use page mode timings. Before 3 Volt Intel StrataFlash memory's page mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set using the Set Read Configuration Register command. For more information on the RCR bits see the *3 Volt Intel® StrataFlash™ Memory:28F128J3A, 28F640J3A, 28F320J3A* datasheet.

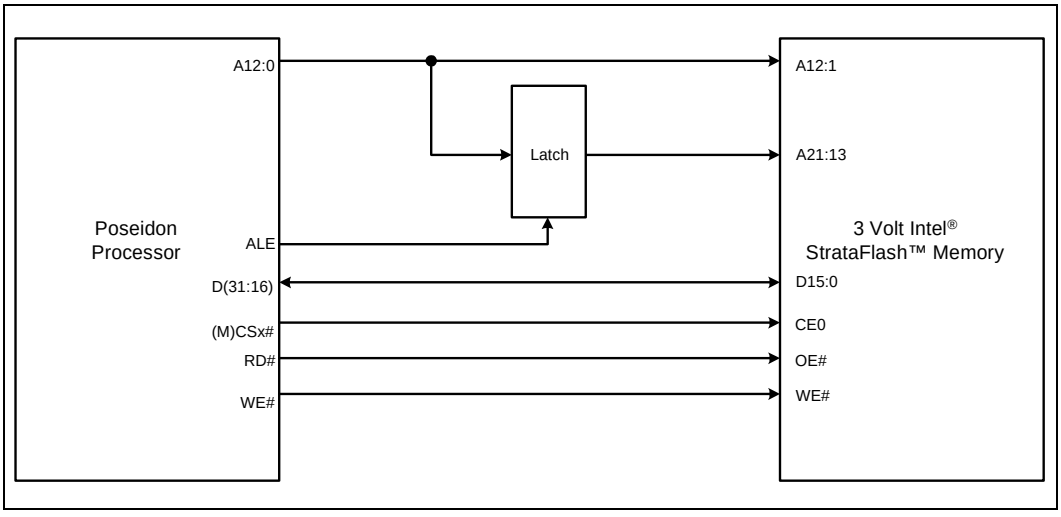
3.0 Interfacing 3 Volt Intel® StrataFlash™ Memory to MIPS PR31700 Poseidon Processor by Philips

The Poseidon processor by Philips is based on a MIPS R3000 core. The PR31700 core runs at a speed of 74 MHz, and is pin-to-pin compatible with the PR31500. The Poseidon Processor includes such features as 4 KB of instruction cache, 1 KB of data cache, and a built-in memory controller.

3.1 Interface Considerations

The Philips PR31700 processor and the 3 Volt Intel StrataFlash memory can interface with only an address latch. The Philips PR31700 processor can be programmed to generate wait-states, eliminating the need for external wait-state logic. It also internally decodes the address bus to generate chip select signals, which can be directly connected to the 3 Volt Intel StrataFlash memory's chip enable signal. Both the processor and the flash can be powered from and interface at 3.3 V. Figure 1 is a block diagram of the interface.

Figure 1. 0.25 µm 3 Volt Intel® StrataFlash™ Memory/Poseidon Interface



3.2 Processor Interface Signals

This interface uses the following signals provided by the Philips PR31700 processor:

$A_{12:0}$: The multiplexed address bus provides addresses to memory. It must be latched to generate the full address.

$D_{15:0}$: The upper half of the 32-bit data bus. This is the portion used for connections to 16-bit memory.

ALE: Address Latch Enable is used as the latch control to generate the upper address bits.

(M)CSx#:CSx# and MCSx# are chip select signals generated by the Philips PR31700 processor.

WE#: Indicates writes from the processor to the system.

RD#: Indicates reads from the processor to the system.

Documentation on the Poseidon processor indicate active low signals with a "/" or a "*." For consistency within this document, the active low signals from the Poseidon processor are indicated with a "#" symbol.

3.3 Controlling the Interface

The memory configuration registers in the Poseidon processor should be set as necessary for proper operation. This includes setting the bus width, the access time for the flash, and enabling page mode for the memory region containing the 3 Volt Intel StrataFlash memory. Page mode should be enabled on the 3 Volt Intel StrataFlash memory before it is enabled on the Poseidon Processor so that invalid data is not read.

The Poseidon processor and the 3 Volt Intel StrataFlash memory both use a four-word page. During bursts, the Poseidon processor always makes consecutive accesses starting on a 16-byte boundary. This means that the Poseidon processor will not cross a page boundary on the 3 Volt Intel StrataFlash memory without inserting necessary wait-states.

Note: The PR31700 processor datasheet does not give abbreviated names for timing specifications. Table 1 shows the symbols used in Figure 3 and Figure 4 and their description from the datasheet.

Table 1. Poseidon Processor Bus Timing Names

Symbol	Description
t_{AV}	Delay DCLKOUT to A[12:0]
t_{DS}	D[31:16] to DCLKIN Setup time
t_{DH}	D[31:16] to DCLKIN Hold time
t_{ALE}low	Delay DCLKOUT to ALE (Rising)
t_{ALE}high	Delay DCLKOUT to ALE (falling)
t_{RD}low	Delay DCLKOUT to RD# (falling)
t_{RD}high	Delay DCLKOUT to RD# (rising)
t_{CS}low	Delay DCLKOUT to CS3-0# (falling)
t_{CS}high	Delay DCLKOUT to CS3-0# (rising)
t_{DV}	Delay DCLKOUT to D[31:16]
t_{WE}low	Delay DCLKOUT to WE# (falling)
t_{WE}high	Delay DCLKOUT to WE# (rising)

Figure 2 is a timing diagram of the 3 Volt Intel StrataFlash memory and the Poseidon processor with page mode reads. DCLKOUT runs at 73.728 MHz, and is what all timing specifications from the PR31700 processor are given off of. The number of wait-states to be used is counted as one less than the number of CLK cycles that an access takes. The diagram shows ALE pulsing high so that the upper addresses can be latched. After the upper addresses are latched and $A_{12:0}$ become valid, the time t_{AVQV} must pass before data is valid. For the second, third and fourth accesses, the time t_{APA} passes before data from the 3 Volt Intel StrataFlash memory is valid.

Figure 2. 3 Volt Intel® StrataFlash™ Memory/Poseidon Processor Page Mode Reads

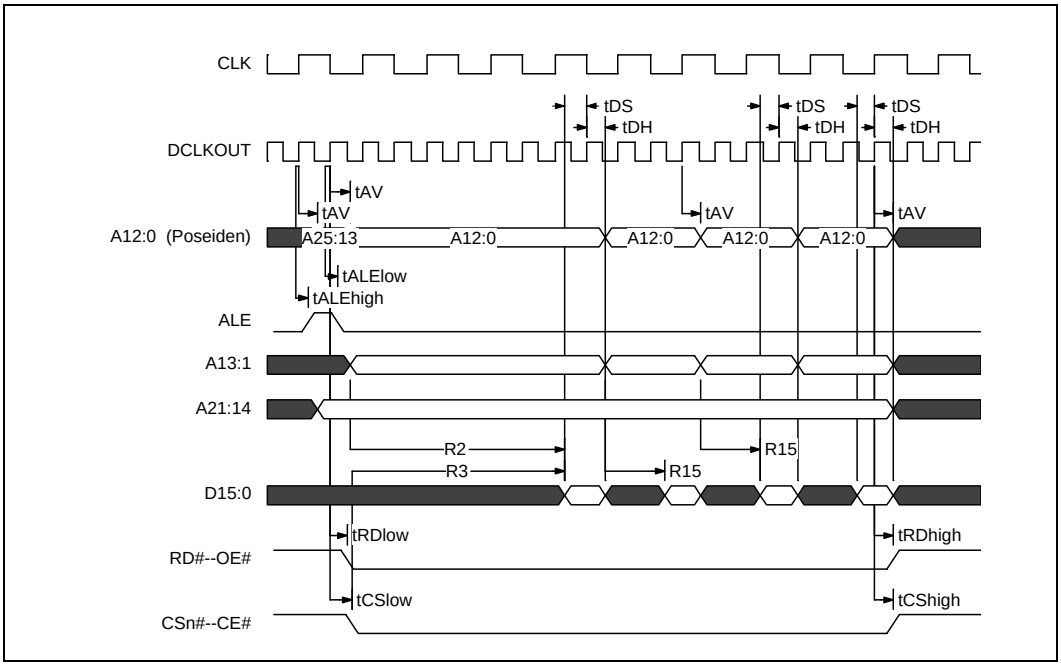
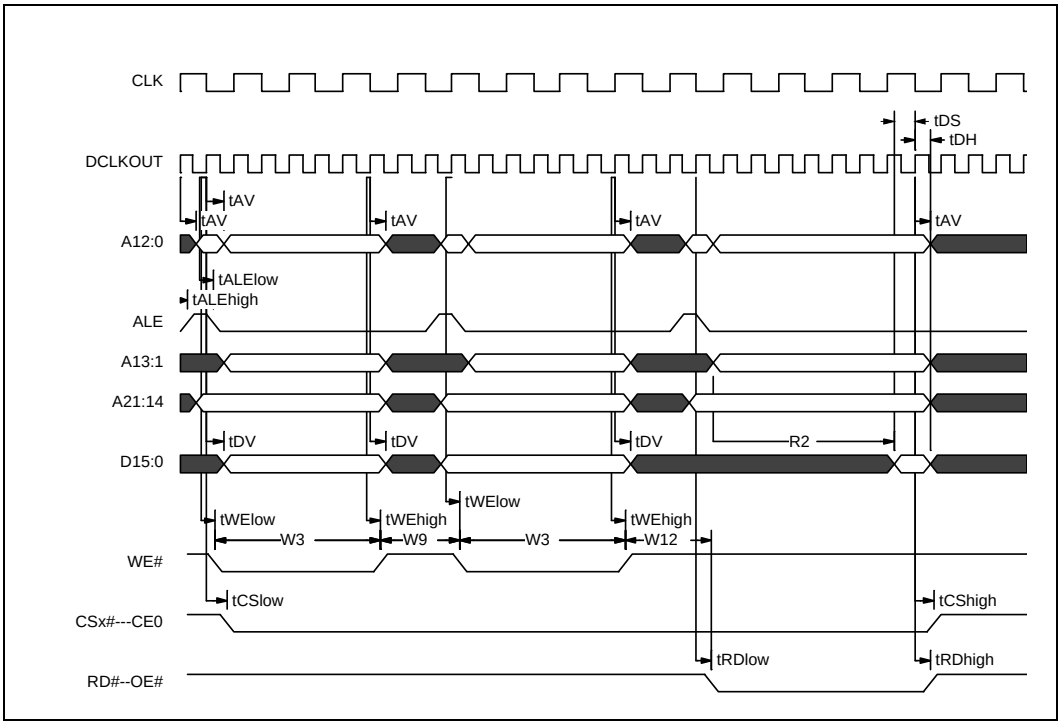


Figure 3 is a timing diagram of two writes followed by a read. WE# is held low long enough to meet the Write Pulse Width time (t_{WP}). When it goes high, the address and data is latched. In between write cycles, WE# must remain high for at least t_{WPH}. This is the reason a clock cycle is left between the writes. For a similar reason, a clock cycle is left between the read and the write. This is to meet the write recovery before read time, t_{WHGL}.

Figure 3. 3 Volt Intel® StrataFlash™ Memory/Poseidon Write Cycles Followed by Read



Several considerations must be taken into account when resetting or powering on the 3 Volt Intel StrataFlash memory. When resetting, RP# must remain low for at least a time of t_{PLPH} (35 µs). In addition, the first output is not valid until 310 ns (t_{PHQV} + t_{PHRH}) after RP# goes high. The PR31700 processor has many power management features, and depending on how these are used with the 3 Volt Intel StrataFlash memory, t_{PLPH} (35 µs) and t_{PHQV} + t_{PHRH} (310 ns) may need to be taken into consideration. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page mode.

The 3 Volt Intel StrataFlash memory can only be used in certain regions of the Poseidon processor's memory map. Regions designated for memory not compatible with flash should not be used to interface with the 3 Volt Intel StrataFlash memory. A memory map of is available in Poseidon processor user's manual. If it is desirable to boot from the 3 Volt Intel StrataFlash memory, then it should be placed in the CS0 region, which is designated for boot ROM. It is mapped starting at address 11000000h in kernel space, while the boot vector location is mapped at address 1FC00000h.

Consult all appropriate datasheets and manuals before attempting this interface (see Appendix A for a list of additional information).

4.0 Summary

3 Volt Intel StrataFlash memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page mode reads. Interfaces between 3 Volt Intel StrataFlash components and various processors can generally be accomplished with a PLD to generate wait-states and WE#, and a decoder to generate chip enable signals. 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different V_{CCQ} voltages. 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. 3 Volt Intel StrataFlash memory is an excellent option for code and data applications where high density and low cost are required.

Appendix A Additional Information

Order Number	Document/Tool
290667	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A* datasheet
298130	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A Specification Update*
297859	*AP-677 Intel® StrataFlash™ Memory Technology*
292222	*AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture*
292221	*AP-663 Using the Intel® StrataFlash™ Memory Write Buffer*
292218	*AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292172	*AP-617 Additional Flash Data Protection Using V_{PP}, RP#, and WP#*

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at http://developer.intel.com/design/flash/isf.