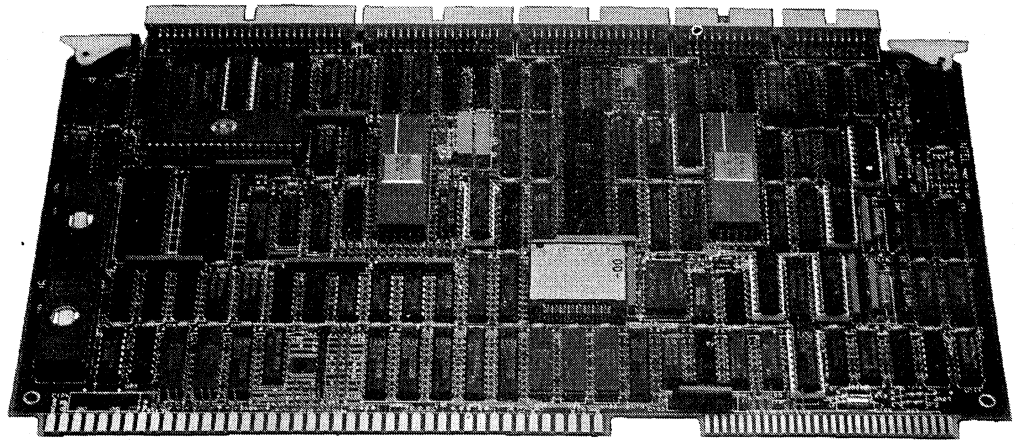
iSBC® 214
PERIPHERAL CONTROLLER SUBSYSTEM

- **Based on the 80186 Microprocessor**
- **Controls up to Two ST506/412 5¼" Winchester Disk Drives**
- **Controls up to Four Single/Double Sided and Single/Double Density 5¼" Flexible Disk Drives**
- **Controls up to Four QIC-02 Streaming Tape Drives**
- **Supports 20 or 24-Bit Addressing**
- **On-Board Diagnostics and Winchester ECC**
- **Incorporates Track Caching to Reduce Winchester Disk Access Times**
- **iRMX™ and XENIX* Operating System Support**

The iSBC 214 Subsystem is a single-board, multiple device controller that interfaces standard MULTIBUS® systems of three types of magnetic storage media. The iSBC 214 Peripheral Controller Subsystem supports the following interface standards: ST506/412 (Winchester Disk), SA 450/460 (Flexible Disk), and QIC-02 (¼" Streaming Tape).

The board combines the functionality of the iSBC 215 Generic Winchester Controller and the iSBC 213 Data Separator, the iSBX™ 218A Flexible Disk Controller, and the iSBX 217C ¼" Tape Drive Interface Module. The iSBC 214 Subsystem emulates the iSBC 215G command set, allowing users to avoid rewriting their software.

The iSBC 214 Peripheral Controller Subsystem offers a single slot solution to the interface of multiple storage devices, thereby reducing overall power requirements, increasing system reliability, and freeing up backplane slots for addtional functionality. In addition, the new iSBC 214 Subsystem can be placed in a 16 Megabyte memory space.



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*XENIX is a trademark of MICROSOFT Corp.

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The iSBC 214 represents a new Peripheral Controller Subsystem architecture which is designed around a dual bus structure and supported by real-time, multitasking firmware. The 80186 controls the local bus and manages the interface between the MULTIBUS and the controller. It is responsible for high speed data transfers of up to 1.6 megabytes per second between the iSBC 214 Subsystem and host memory. The 80186 and the multitasking firmware decode the command request, allocate RAM buffer space, and dispatch the tasks.

A second bus, the I/O Transfer Bus, supports data transfers between the controller and the various peripheral devices. It is this dual bus system that allows the iSBC 214 Subsystem to provide simultaneous data transfers between the controller and the storage devices, and between the controller and the MULTIBUS. (See Figure 1).

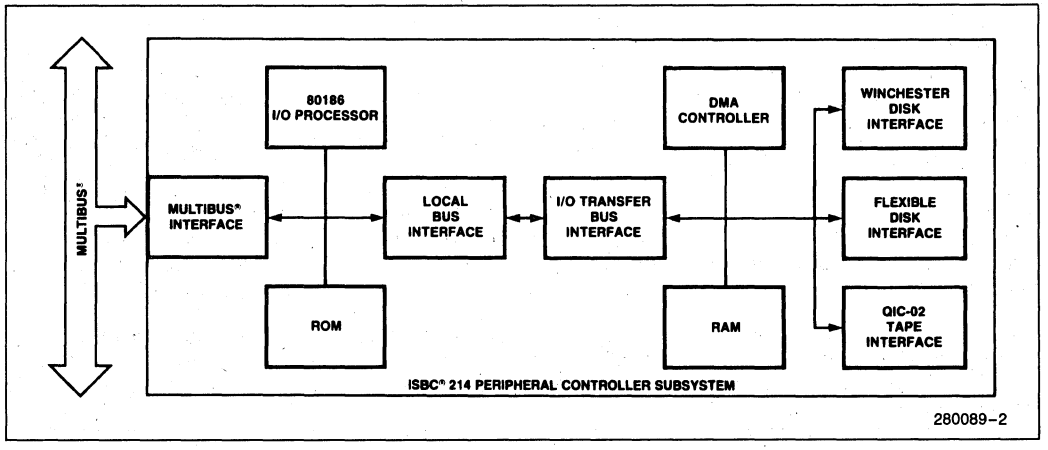

Figure 1. Block Diagram iSBC® 214 Peripheral Controller Subsystem

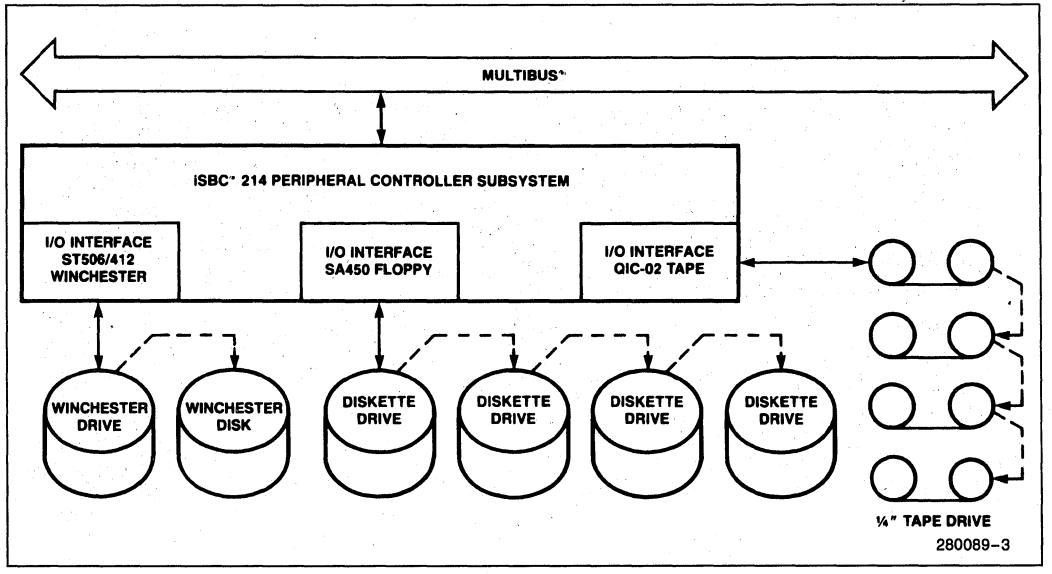

Figure 2. Fully Configured Peripheral Subsystem

The iSBC 214 Subsystem implements an intelligent track caching scheme through dynamic allocation of buffer space. This provides reduced access times to the Winchester disk and improved system performance. Operating systems with file management designed to handle sequential data can be supplied directly from the cache without incremental access to the disk.

FUNCTIONAL DESCRIPTION

Winchester Disk Interface

The iSBC 214 Subsystem provides control of one or two ST506/412 compatible Winchester devices and supports up to 16 Read/Write heads per drive. The Intel 82062 acts as the main controller taking care of FM/MFM encoding and decoding, bit stream serialization and deserialization, address mark detection and generation, sector identification comparisons, CRC error checking and format generation. The board uses a standard daisy-chained control cable and a separate data transfer cable for each device supported.

ECC

High data integrity is provided by on-board Error Checking Code logic. For burst error correction, a 32-bit code is appended to the sector data fields by the controller. During a read operation, the same logic regenerates the ECC polynomial and compares this second code to the appended ECC. The ECC logic can detect an erroneous data burst up to 32 bits in length with correction up to 11 bits.

If an ECC error is detected the controller automatically initiates a retry operation on the data transfer. If the maximum retry count is exceeded, the location of the bad data within the transfer buffer is identified and the 80186 then performs error correction on the data bytes.

Flexible Disk Interface

The Flexible Disk Controller performs all data separation, FM (single density) and MFM (double density) encoding, and CRC support. The 34-pin connector is designed to support the SA450/460 interface directly and up to four flexible disk devices may be connected to the controller.

Tape Controller Interface

The tape controller section of the iSBC 214 Subsystem is based on the 8742 Universal Peripheral Interface (UPI). It is capable of supporting up to four QIC-02 compatible streaming tape drives over a standard 50-pin daisy-chained cable.

All standard QIC-02 commands are supported. All drives must be capable of streaming at 30 or 90 inches per second.

MULTIBUS® Host Interface

The MULTIBUS connection consists of two standard printed circuit board edges that plug into MULTIBUS edge connectors on a backplane in the system bus. An active P1 connector is required and serves as the Host systems's communciation channel to the controller. An active P2 connector is optional and only required for supporting full 24-bit addressing and power fail signals.

SPECIFICATIONS

Compatibility

CPU—any iSBC MULTIBUS computer or system mainframe.

Winchester disk—Any ST506/412 compatible, 5.25″ disk drive.

Flexible disk—Any SA450/460 compatible, 5.25″ disk drive.

Tape drive—Any QIC-02 compatible, .25″ streaming tape drive.

Controller-to-drive cabling and connectors are not supplied with the controller. Cables can be fabricated with flat cable and commercially-available connectors as described in the iSBC 214 Hardware Reference Manual.

Physical Characteristics

Width: 6.75 in. (17.15 cm)
Height: 0.5 in. (1.27 cm)
Length: 12.0 in. (30.48 cm)
Shipping Weight: 19 oz. (540 g)

Ordering Information

iSBC 214 Peripheral Controller Subsystem.

Mounting: Occupies one slot or SBC system chassis or cardcage/backplane.

Electrical Characteristics

Power Requirements: +5 VDC @ 4.5A max.

Environmental Characteristics

Temperature: 10°C to 55°C with airflow of 200 linear feet per minute (operating); −55°C to +85°C (non-operating).

Humidity: Up to 90% relative humidity without condensation (operating); all conditions without condensation or frost (non-operating).

Reference Manual

134910-001: iSBC 214 Peripheral Controller Subsystem Hardware Reference Manual (not supplied). Reference Manual may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.