



Upgrading Designs from the 3.3 V, 5 V Tolerant 80960JA/JF/JD Embedded Processors to the 80960JT

White Paper

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Contents

1.0	Abstract	1
2.0	Summary	1
3.0	References	2
	3.1 Document/Order Number/WWW Address	2
4.0	Software Conversion Issues	2
	4.1 Code Compatibility	2
	4.2 Device ID	2
	4.3 Synchronizing Code Execution With External Events.....	3
	4.4 On-Chip Timers.....	3
	4.5 Instruction Cache	3
	4.6 Data Cache	4
	4.7 Interrupts.....	4
	4.8 Faults	4
	4.9 System Initialization and Boot-Up.....	4
5.0	Hardware Conversion Issues	4
	5.1 Core Clock Multiple.....	4
	5.2 External Bus Timings and Bus Frequency.....	5
	5.3 Power Supply and Decoupling Requirements	5
	5.4 I/O Voltages	5
	5.5 Thermal Issues	5
	5.6 Packages	5
	5.7 JTAG Boundary Scan Chain.....	6
	5.8 LCD-960 Debug Feature.....	6
	5.9 Input/Output Buffer Information Specification (IBIS) Modeling	6

Figures

No Figures used

Tables

1	White Paper Topics.....	1
2	80960Jx Instruction Cache Sizes.....	3
3	80960Jx Data Cache Sizes.....	4

1.0 Abstract

This white paper summarizes the issues to consider when upgrading an application design from the 80960JA, 80960JF, or 80960JD embedded processors to the 80960JT. The increased execution speed of the 80960JT can affect application behavior in unexpected ways. This paper delves into those less obvious affects. Software and hardware design concerns are covered.

Except where noted otherwise in this paper, the 80960JT is identical to the 80960JA/JF/JD processors.

All comments in this paper relate to a 3.3 V, 5 V tolerant 80960JA, 80960JF, or 80960JD processor upgrade to the 80960JT. See [Section 3.0, “References” on page 2](#) for other documents that discuss conversions from other versions of the 80960JA, 80960JF or 80960JD to the 3.3 V, 5 V tolerant versions.

This paper does not replace the technical descriptions of the 80960JA, 80960JF, 80960JD, and 80960JT processors. Consult the most recent 80960Jx processor data sheet and developer’s manual for design details for these processors.

2.0 Summary

The 80960JT processor is essentially a clock-tripled version of the 80960JD with larger instruction and data caches. The typical motivation for upgrading an application to the 80960JT is to take advantage of the increased processing performance.

Performance benefits can be evaluated easily in existing 80960JA/JF/JD applications. The 80960JT is a code- and pinout-compatible drop-in replacement for the 3.3 V, 5 V tolerant line of 80960JA/JF/JD processors. The 80960JT external bus timings match the 80960JD. The 80960JT power consumption and thermal ambient requirements are within 10% and 5°C, respectively, of the 80960JD for the same bus frequency and package.

An application’s actual performance improvement is limited primarily by the available external bus bandwidth of the 80960JA/JF/JD design. External bus bandwidth can be improved through effective use of the larger on-chip caches of the 80960JT.

The 80960JT also offers a new debugging feature (Low Cost Debugger, or LCD-960) through the JTAG Boundary Scan serial port pins.

The topics of this paper are organized in [Table 1](#).

Table 1. White Paper Topics

Software Topics	Page	Hardware Topics	Page
Code Compatibility	2	Core Clock Multiple	4
Device ID	2	External Bus Timings and Bus Frequency	5
Synchronizing Code Execution With External Events	3	Power Supply and Decoupling Requirements	5
On-Chip Timers	3	I/O Voltages	5
Instruction Cache	3	Thermal Issues	5
Data Cache	4	Packages	5
Interrupts	4	JTAG Boundary Scan Chain	6
Faults	4	LCD-960 Debug Feature	6
System Initialization and Boot-Up	4	Input/Output Buffer Information Specification (IBIS) Modeling	6

3.0 References

3.1 Document/Order Number/WWW Address

- *i960[®] Jx Microprocessor Developer's Manual*
272483
<http://www.intel.com/design/i960/manuals/272483.htm>
- *80960JA/JF/JD/JT 3.3 V Embedded 32-Bit Microprocessor Data Sheet* (All the 3.3 V, 5 V tolerant 80960Jx data sheets have been merged into one document. This data sheet obsoletes all previous versions)
273159
<http://www.intel.com/design/i960/datashts/273159.htm>
- *80960Jx Processor Specification Update*
272852
<http://www.intel.com/design/i960/specupdt/272852.htm>
- *5 V 80960JA/JF/JD Processor Conversion to 3.3 V (5 V to 3.3 V 80960Jx Conversion Paper)*
273172
<http://www.intel.com/design/i960/applnots/273172.htm>
- *80L960JA/JF Processor Conversion to 80960Jx 3.3 V, 5 V Tolerant Processor (3.3 V-only to 3.3 V, 5 V Tolerant Conversion Paper)*
273167
<http://www.intel.com/design/i960/applnots/273167.htm>

4.0 Software Conversion Issues

4.1 Code Compatibility

The instruction set is identical between the 80960JA/JF/JD processors and the 80960JT. The function and location of all unreserved registers, flags, tables, queues, address modes and data types are the same for all 80960Jx processors. The boot up sequence is also common among the 80960Jx family members.

4.2 Device ID

Not surprisingly, a new device like the 80960JT receives a unique device identification (ID) code. Software that recognizes the processor device identification must be revised to accept the 80960JT ID code. See the *80960JA/JF/JD/JT 3.3 V Embedded 32-Bit Microprocessor Data Sheet* (details provided in [Section 3.0, "References" on page 2](#) of this paper) for the correct ID codes.

4.3 Synchronizing Code Execution With External Events

Any software that relies on the processor execution speed to synchronize with external events or bus masters must be evaluated with the 80960JT since the processing speed is higher. For example, a carefully timed DRAM refresh cycle that fits between accesses on a 80960JA/JF/JD might contend and produce a system crash on the 80960JT. Whenever possible, use a hardware timer (such as the two internal 32-bit timers on all 80960Jx processors), an external interrupt, or the bus arbitration signals to synchronize code execution with external events.

4.4 On-Chip Timers

All 80960Jx processors feature two 32-bit timers. In all cases, the timers operate at the external bus frequency, so they keep consistent time regardless of the internal clock multiple. All control registers for the timers are identical across the 80960Jx processor family.

4.5 Instruction Cache

The 80960JT on-chip instruction cache is larger than on any 80960JA/JF/JD processor, as shown in [Table 2](#) below. The cache topologies are the same, in that all are 2-way, set associative, employ a write through update policy, and they support locking code into half the cache.

Table 2. 80960Jx Instruction Cache Sizes

80960Jx Processor	80960Jx Instruction Cache Size
80960JA	2 Kbytes
80960JF	4 Kbytes
80960JD	4 Kbytes
80960JT	16 Kbytes

Since the larger cache on the 80960JT can contain more instructions, larger portions of the application program can execute from cache. The cache effectiveness relies heavily on the size and associativity of the application code, of course. More code executing from cache can mean faster processing and less code fetching from external memory, thus relieving the external bus bandwidth bottleneck.

4.6 Data Cache

The 80960JT data cache is larger than on the 80960JA/JF/JD processors as shown in [Table 3](#), below. The cache topologies are the same, in that all are direct mapped and employ a write through update policy.

Table 3. 80960Jx Data Cache Sizes

80960Jx Processor	80960Jx Data Cache Size
80960JA	1 Kbytes
80960JF	2 Kbytes
80960JD	2 Kbytes
80960JT	4 Kbytes

The larger 80960JT cache allows more data to remain cached on-chip for faster access and reduced traffic on the external address/data bus. Again, the cache effectiveness relies heavily on the size and associativity of the application data.

4.7 Interrupts

Since the 80960JT executes code faster than the 80960JA/JF/JD processors, interrupt service routines (ISRs) can execute in less time, especially if the interrupt service routines are locked into the instruction cache. Especially in the case of level-sensitive interrupts, an ISR can conclude before the external interrupt signal retires and trigger an unwanted interrupt.

4.8 Faults

Similar to interrupts, fault handlers can execute in less time on the 80960JT than on the 80960JA/JF/JD processors.

4.9 System Initialization and Boot-Up

Functionally, the 80960JT boots up and initializes exactly like the 80960JA/JF/JD processors. The time required to complete the built-in self test is a function of the internal execution speed and the size of the caches being tested. See the "Cold Reset Waveform" in the *80960JA/JF/JD/JT 3.3 V Embedded 32-Bit Microprocessor* Data Sheet for more details.

5.0 Hardware Conversion Issues

5.1 Core Clock Multiple

The 80960JT processor operates internally at three times the external bus frequency. This higher clock multiple may affect the electromagnetic conformance (EMC) signature of the application. Otherwise, depending on the available external AD31:0 bus bandwidth, code can execute up to 50% faster on the 80960JT than on a 80960JD.

5.2 External Bus Timings and Bus Frequency

The 80960JT bus timing specifications – input setup, input hold, output valid, and output hold – are identical to the 80960JD. The 80960JA/JF bus timing specifications are also being revised to match the 80960JD. The 80960JT minimum clock frequency is higher than for the 80960JD because the 80960JT phase-locked loop (PLL) stability becomes unacceptable at lower frequencies. Consult the *80960JA/JF/JD/JT 3.3 V Embedded 32-Bit Microprocessor Data Sheet* (see [Section 3.0](#), “References” on page 2 of this paper) for more details.

5.3 Power Supply and Decoupling Requirements

The 80960Jx processors covered in this paper operate from a 3.3 V V_{CC} supply. The 80960JT dissipates about 10% more power than the 80960JD at the same frequency. A 50% increase (100 MHz vs. 66 MHz) in processing speed at 10% more power means the 80960JT design is more power efficient than the 80960JD processor.

Like the 80960JA/JF/JD, the 80960JT supports HALT mode to save power during idle times. If HALT mode is to be employed, use a fast response voltage regulator to prevent voltage spikes when the I_{CC} current drops or rises suddenly.

High frequency decoupling capacitance requirements remain important for the 80960JT. The 80960JT in the 132-lead PQFP package provides separate pins for $V_{CC}(\text{Core})$ and $V_{CC}(\text{I/O})$ which should be decoupled separately, like on the 80960JA/JF/JD. $V_{CC}(\text{Core})$ provides power to the processor core logic while $V_{CC}(\text{I/O})$ supports the input and output pins that can produce high switching transients by toggling large external capacitive loads.

5.4 I/O Voltages

The 80960JA/JF/JD and the 80960JT processors support 3.3 V, 5 V-tolerant input and output signals. In all cases, the VCC5 pin voltage must be at least as high as the highest input voltage.

5.5 Thermal Issues

The maximum ambient temperature for the 80960JT is only about 5°C lower than for the 80960JD at the same bus frequency. The 80960JT shares the same maximum case temperature as the 80960JD. Consult the *80960JA/JF/JD/JT 3.3 V Embedded 32-Bit Microprocessor Data Sheet* (see [Section 3.0](#), “References” on page 2 of this paper) for more details.

5.6 Packages

The 80960JA/JF/JD and 80960JT come in ceramic pin grid array (PGA) and plastic quad flatpack (PQFP) packages. Pin counts and pin definitions are identical among the 80960Jx family.

Moreover, the 80960Jx processors covered in this paper come in the new plastic ball grid array (PBGA) with a significantly smaller footprint (15 mm x 15 mm) and height (1.8 mm) than the other packages for space constrained applications.

5.7 JTAG Boundary Scan Chain

All the 80960Jx processor share a common JTAG Boundary Scan chain. JTAG vectors written for the 80960JA/JF/JD also work for the 80960JT. The scan chain appears in the *80960JA/JF/JD/JT 3.3 V Embedded 32-Bit Microprocessor Data Sheet*. Electronic copies of the scan chain (in Boundary Scan Description Language (BSDL) format) are available on the Web at:

<http://www.intel.com/design/i960/swsup/>

5.8 LCD-960 Debug Feature

The 80960JT supports the Low Cost Debugger (LCD-960), a new debug feature not found on the 80960JA/JF/JD. The LCD-960 capability permits users to download code, interrogate and write to internal registers and external memory, set runtime breakpoints, disassemble execution code, single-step through code, and more through the JTAG serial communication port. Developers can debug software on the application itself without the necessity of a PGA socket or a high-priced emulator. Access to the 80960JT JTAG serial port pins and a relatively low-cost interface system from third party vendors is all it takes.

5.9 Input/Output Buffer Information Specification (IBIS) Modeling

The analog parameters for the inputs and outputs (in standard “IBIS” format) are available. IBIS models are used to predict the analog behavior of the input and output pins. The models are available on the Web at:

<http://www.intel.com/design/i960/swsup/>